Thoughts on Intel® Xeon® E5-2600 v2 Product Family Performance Optimisation – component selection guidelines

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Romley EP/EN Platforms
Intel® Xeon® Processor E5-2600 v2/2400 v2 Product Families

Ivy Bridge CPUs
Socket R: Up to 12 cores / socket
Socket B2: Up to 10 cores / socket

Memory
DDR3 & DDR3L
RDIMMs & UDIMMs, LR DIMMs
Socket R: 4 channels per socket, up to 3 DPC; speeds up to DDR3 1866
Socket B2: 3 channels per socket, up to 2 DPC; speeds up to DDR3 1600

Intel® LOM Options
1GbE: Hartwell
Powerville
10GbE: Twinville (10GBase-T)
Niantic (SfI/KR)

Intel® C600 series chipset (Patsburg PCH)
Optimized Server & WS PCH
Integrated Storage:
Up to 8 ports 3Gb/s SAS
RAID 5 optional

Intel® Xeon® processor E5-2400/2600 prod fam
Socket R: 2 QPI links
Socket B2: 1 QPI link

Intel® Xeon® processor E5-2400/2600 prod fam
QPI

Intel® C600 series chipset
3Gb/s SAS, SATA

PCI Express* 3.0
Socket R: 40 lanes per socket
Socket B2: 24 lanes per socket
Extra Gen 2 x4 on 2nd CPU

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Intel® Xeon® Processor E5-2600 v2 Product Family

**Advanced**
- 8C-20MB, 10C-25MB cache
- 8.0 GT/s QPI
- Intel® HT Technology
- DDR3-1866 (skt R)
- Intel® Turbo Boost Technology

**Standard**
- 6C-15MB, 8C-20MB cache
- 7.2 GT/s QPI
- Intel® HT Technology
- DDR3-1600
- Intel® Turbo Boost Technology

**Basic**
- 4C-10MB, 2C-5MB cache
- 6.4 GT/s QPI
- DDR3 1333

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**Segment Optimized**
- 2.5MB/c cache
- 8C, 2.5GHz
- Intel® HT Technology
- DDR3-1866
- Intel® Turbo Boost Technology

**Low Power**
- 2.5MB/c cache
- 10C, 8.0 GT/s QPI
- Intel® HT Technology
- DDR3-1600
- Intel® Turbo Boost Technology

**Tray only SKUs**

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- Tray only SKUs
Q1: What are the key performance differences on 12C & 10C E5-2600 v2 SKUs?

There are 3 key differences that affect performance:

1. Number of Memory Controllers
   - 12C SKUs have 2 memory controllers, all other SKUs have 1 memory controller
   - The 2nd memory controller gives a 3-4% improvement in memory bandwidth
   - More details provided in: Intel Xeon Processor E5 Family Romley Memory Config Guide

2. Turbo Frequencies
   - Top-bin 10C part (E5-2690 v2) has a higher max frequency than the 12C SKUs
   - Frequency remains higher for top-bin 10C vs. 12C SKUs at low core counts

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1 Source: Intel internal measurements as of Sept 2013 on STREAM Triad v5.4. E5-2697 v2, 8x16GB DR-DDR3-1866 DIMMS vs. E5-2690 v2, 8x16GB DR-DDR3-1866 DIMMS. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to http://www.intel.com/performance
Q1: What are the key performance differences on 12C & 10C E5-2600 v2 SKUs?

3. Last Level Cache (LLC) Latency
   - At the same frequency, 12C SKUs have 20% higher LLC latency than 10C SKUs
   - Differences in LLC latency are due to the die configurations
     - 12C die has 3 columns of cache & core, with the 3rd column adding to LLC latency
     - 10C die has 2 columns of cache & core, similar to E5-2600 (SNB-EP)

<table>
<thead>
<tr>
<th>Latency for sequential reads (ns)</th>
<th>LLC Local Memory</th>
<th>Remote Socket Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>E5-2690 v2 (10C, 3.0GHz, DDR3-1866)</td>
<td>13 ns</td>
<td>58 ns</td>
</tr>
<tr>
<td>E5-2697 v2 (12C, 3.0GHz, DDR3-1866)</td>
<td>16 ns</td>
<td>61 ns</td>
</tr>
</tbody>
</table>
Q2: At low thread counts, how does performance differ on 12C & 10C E5-2600 v2 SKUs?

- When software doesn’t have enough threads to take advantage of extra cores, performance is more sensitive to memory latency & frequency.

- At low thread counts, 10C SKUs may have the performance advantage over 12C SKUs due to lower LLC latencies & higher turbo frequencies.
Q3: What is difference in the memory bandwidth of DDR3 DIMMs running at 1866 MHz compared to 1600 MHz?

- With all cores enabled, there is up to 12.5% increase in memory bandwidth on E5-2697 v2 using DDR3-1866 MHz vs. DDR3-1600 MHz DIMMs.
  - More details provided in: Intel Xeon Processor E5-2600 v2 Product Family Performance

- When not all cores are active, the full 12.5% increase in memory bandwidth from 1866 MHz DIMMs may not be provided.
  - There is a limitation on the number of memory transactions that can be issued by each core. When only a few cores are active, there are not enough memory transactions to saturate the memory controller and take advantage of the higher frequency.
Memory Latency & Bandwidth
Faster Memory, Better Efficiency, Similar Latency

Internal latency/bandwidth tool
66% Reads, 33% writes (RFO)
Windows 2008 R2 SP1
E5-2697 v2, 12C, turbo enabled @ 3.0GHz [July 2013]
E5-2690, 8C, turbo enabled @ 3.1GHz [Sept 2011]
1 dual-ranked RDIMM per channel, 4 channels (varied DDR frequencies),
Pre-production BIOS, All threads active (HT)

Up to 12.8% more efficient
Up to 20% bandwidth increase
Up to 12.5% from DIMM frequency increase

Similar loaded/idle latencies despite core count growth

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.
Platform Memory Overview
(Intel® Xeon® processor E5-2600 Product Family)

• Platform capability (up to 24 DIMMs):
  − Up to 4 memory channels per CPU
  − Up to 3 DIMMS per channel

• Memory types supported:
  − DDR3 1866 (v2 only), 1600, 1333, 1066, and 800
  − 1.5V and 1.35V DIMMs (1.35V = LV = Low Voltage)
  − Registered (RDIMM), Unbuffered (UDIMM) & LR (Load Reduced)
    − Mixing of UDIMM, RDIMM or LR-DIMMS is NOT supported
  − 1Gb, 2Gb & 4Gb memory technologies
  − Single-rank (SR), dual-rank (DR), quad-rank (QR)
    − QR DIMMs limited to 2 DPC and only 800 or 1066MHz

• System memory speed (i.e. the speed at which the memory is actually running) is set by BIOS depending on:
  − CPU capability
  − DIMM type(s) used (memory speed, U/RDIMM, SR/DR/QR)
  − DIMMs populated per channel
  − See subsequent foils for exact configurations supported (Speed, # of DIMMS etc.)

• All memory channels in a system will run at the slowest common frequency
Memory Configuration Definitions

**Balanced**

- All DIMMs Identical: Yes
- All Memory Channels Populated: Yes
- All Channels Identically Populated: Yes

**Un-balanced**

- All DIMMs Identical: Maybe
- All Memory Channels Populated: Maybe
- All Channels Identically Populated: No

**Near-Balanced**

- All DIMMs Identical: No
- All Memory Channels Populated: Yes
- All Channels Identically Populated: Yes
Optimizing for Memory Performance: General Guidelines and Priorities

1. Use identical DIMM types throughout the platform:
   - Same size, speed, and number of ranks

2. Maximize number of channels populated for highest bandwidth

3. Use a “balanced” platform configuration:
   - All available memory channels populated equally
   - Identical DIMMs in all locations (size/speed/rank)

4. Use a “near-balanced” platform configuration:
   - All available memory channels and sockets populated equally
   - Identical DIMMs in each “row”, but different sized DIMMs in row #1 vs. row #2

5. For performance...use Dual Rank DIMMs (DR) then SR or LR-DIMMs
   - Use QR DIMMs as a last option (the memory bus will run slower with QR DIMMs)
Guidance to using Memory Performance Data

- Not all applications are equally sensitive to memory performance (in particular memory bandwidth)
  - Some applications are highly sensitive (typically HPC, Financial)
  - Some are moderately sensitive (Virtualization, Web)
  - And some are relatively insensitive (Database)
- The information provided here favors applications that are moderately to highly sensitive to memory bandwidth
  - As such, the info here may not be applicable to all situations
    - E.g. database applications are sensitive to memory capacity and latency, and not so much to memory bandwidth. As such, database apps will typically get more performance out of larger capacity memory configurations, even if such a configuration is identified as lower performance here
- In addition, the performance difference between one configuration and another may be relatively small, but the cost of such a configuration is relatively large.

Use the data here as a guide; apply appropriately to your situation
Q4: What type of DIMMs should be used in E5-2600 v2 systems for the best memory bandwidth?

For best performance, use pTRR compliant DDR3 DIMMs and enable the pTRR feature.

- When non-pTRR compliant DIMMs are used, the E5-2600 v2 system defaults into double refresh mode, which has longer memory latency/DIMM access latency and can lower memory bandwidth by up to 2-4%.

- As a debug option only, disable the penalty of double refresh mode for non-pTRR DIMMs by setting:
  - Advanced->Memory Configuration->Memory RAS Configuration
  - DRAM Maintenance -> Manual
  - Note: Intel does not recommend this setting in production systems since this exposes the DDR3 pass gate issue that can lead to memory errors

Background:

- DDR3 DIMMs are affected by a pass gate charge migration issue (also known as Row Hammer) that may result in a memory error.

- The Pseudo Target Row Refresh (pTRR) feature introduced on Ivy Bridge processor families (2S/4S E5 v2, E7 v2) helps mitigate the DDR3 pass gate issue by automatically refreshing victim rows.

- More details provided in Doc #522542 – Intro to DDR3 Memory Refresh Management
A7 Address Mode is a new BIOS option introduced on E5-2600 v2 systems.

Enabled by default, A7 Address Mode changes the interleave from the default cache line interleave between channels to a two cache line interleave between channels.

For applications with a cache line stride, the second access is mapped to the same channel as the first access which maps to the same page in memory, resulting in a page hit. A page hit saves multiple cycles of latency, as the page does not need to be opened before it is read.

For example: If a system has 4 memory channels populated with proper channel interleave in A7 Address Mode, a 512-byte stride will send all requests to the same channel.
Q5: What is the recommended setting for A7 Address Mode?

A7 Address Mode should be disabled when three of the memory channels are populated on E5-2400 v2 SKUs or E5-2600 v2 SKUs with less than 12 cores to prevent memory bandwidth degradation in these configurations.

- More details provided in Doc #503836 - Ivy Bridge BIOS Writer’s Guide

### A7 Address Mode Recommendations

<table>
<thead>
<tr>
<th>A7 Address Mode Recommendations</th>
<th># of memory channels populated per socket</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 channel</td>
</tr>
<tr>
<td>E5-2600 v2 Product Family (IVB-EP)</td>
<td>E5-2697 v2 or E5-2695 v2 (12 cores)</td>
</tr>
<tr>
<td>All other E5-2600 v2 SKUs (4,6,8,10 cores)</td>
<td>Default (enable A7)</td>
</tr>
<tr>
<td>E5-2400 v2 Product Family (IVB-EN)</td>
<td>All E5-2400 v2 SKUs</td>
</tr>
</tbody>
</table>

Key: Intel recommended configuration for best performance